REMARKS

This application was filed with 12 claims. Claims 1-12 have been rejected. Claims 1, 4, 6, 9, 10, and 12 have been amended. Therefore, Claims 1-12 are pending in the Application. Reconsideration of the application based on the remaining claims as amended and arguments submitted below is respectfully requested.

Claim Rejections - 35 U.S.C. § 112

Claim 2 has been rejected under U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. In response, Claims 1 and 2 have been amended to point out the invention more clearly and to eliminate any perceived contradiction. On page 8, line 19 through page 9, line 9 of the application, the inventors describe two ways that filter coefficients for the timing loop filter may be selected. The coefficients are determined during the training mode as further described beginning on page 11, line 20 of the specification. Once the coefficients are chosen and are inserted within the timing loop filter structure, the coefficients are not changed. It is well-known by those skilled in the art that a linear equalizer 20 has coefficients that are continually updated. Since the timing loop coefficients are not updated, the timing loop filter is operating independently of the linear equalizer during the data mode.

Applicant respectfully requests that the rejection of Claim 2 under § 112 be withdrawn.

Claim Rejections - 35 U.S.C. § 102(e)

Claims 1, 3, 5, 7 and 10-12 have been rejected under 35 U.S.C. § 102(e) as being anticipated by Yedid (6,240,132). The Office Action refers specifically to Fig. 1 of Yedid. With reference to Fig. 1, the teaching of Yedid (6,240,132) is described as a predictor cancellation technique and not to an equalizer. Yedid does not have an equalizer within his timing loop structure, but has a linear canceller 50 (i.e., a predictor as indicated in col. 2, line 39). The linear canceller of Yedid has two inputs. One of the inputs is a communication signal exiting amplifier 19 and delayed by alignment delay element 51. The second input is coupled from decision block 22 over link 21 to the linear canceller 50. The output of linear canceller element 53 of Yedid is a difference signal provided by element 52 as described by Yedid in col. 2, line 45-60. In contrast the timing equalizer filter of the claimed invention has only a single input and the output is not a difference signal as in Yedid, but a filtered signal exiting the timing loop filter. Nowhere does Yedid disclose, suggest or imply that a timing equalizer filter be placed within the timing loop. Such a limitation is recited in independent Claims 1, 5, and 10-12 as amended and should be allowable over Yedid. Claim 3 is dependent on Claim 1 and Claim 7 is dependent on Claim 5 and should be also allowable.

The rejection of Claims 1, 3, 5, 7 and 10-12 under 35 U.S.C. § 102(e) should be withdrawn.

Claim Rejections - 35 U.S.C. § 103

Claims 4 and 8 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Yedid (6,240,132) in view of Fig. 1 and pages 2-3 of the present application.

Transmitter and receiver pairs used in a data communication system as described in the disclosure of the present invention operate in a training mode and a data mode. The training mode is used when the transmitter and receiver are first installed in a loop and turned on. Once the training mode has been completed – the transmitter/receiver pair typically operates in the data mode for long periods of time. During the training mode the linear equalizer is partially trained and has coefficient values that are a good representation of the loop characteristics at the time of training. However when the transceiver pair operates in the data mode the line conditions change and the linear equalizer is continually updated.

Claim 4 is dependent on Claim 1 and therefore includes the limitation that the timing loop includes a timing equalizer filter. Claim 8 includes the step of "functionally positioning a timing equalizer filter in the timing loop." As demonstrated above, Yedid does not disclose the use of a timing equalizer filter (as described in the specification, for example) within the timing loop. Therefore, Yedid, either alone or in combination with Fig. 1 of the present application, does not teach the inventions of Claims 4 and 8.

Claim 6 has been rejected under 35 U.S.C. 103(a) as being unpatentable over Yedid (6,240,132) in view of Harikumar (6,526,105). Claim 6 is dependent on Claim

5. Claim 5, as amended, includes the step of "operating the timing equalizer filter within the timing loop." Yedid does not have a timing equalizer filter and therefore does teach this step. Harikumar describes a time domain equalization technique for use in discrete multi-tone (DMT) receiver. Harikumar does not teach a timing loop with a timing equalizer filter in a for acquiring and maintaining signal timing between a data communications transmitter and receiver connected at central and remote ends of a communications loop.

Claim 9 has been rejected under 35 U.S.C 103(a) as being unpatentable over Yedid (6,240,132) in view of Fig. 1 and pages 2-3 of the present application, as applied to Claim 8 above and further in view of Harikumar (6,526,105). Claim 9 is dependent on Claim 8. For the reasons discussed above with reference to Claim 8, Claim 9 should be allowable.

Applicant has commented on some of the distinctions between the cited references and the claims to facilitate a better understanding of the present invention. This discussion is not exhaustive of the facets of the invention, and Applicant hereby reserves the right to present additional distinctions as appropriate. Furthermore, while these remarks may employ shortened, more specific, or variant descriptions of some of the claim language, Applicant respectfully notes that these remarks are not to be used to create implied limitations in the claims and only the actual wording of the claims should be considered against these references.

Pursuant to 37 C.F.R. § 1.136(a), Applicant petitions the Commissioner to extend the time for responding to the November 1, 2004, Office Action for one month from February 1, 2005 to March 1, 2005. Applicant encloses herewith a check in the amount of $120.00 made payable to the Director of the USPTO for the petition fee. The Commissioner is authorized to charge any deficiency or credit any overpayment associated with the filing of this Response to Deposit Account 23-0035.

Respectfully submitted,

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CERTIFICATE OF FIRST CLASS MAILING

I hereby certify that this Response and Amendment and a check in the amount of $120.00 are being deposited with the United States Postal Service as first class mail in an envelope addressed to:

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

on March 1, 2005.

Emily A. Shouse

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March 1, 2005
Date